In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended. Claims 4 - 9, 26, 31 and 32 are canceled without prejudice of disclaimer. It is assumed that the amendments to claims 23 and 38 requested in the response filed December 28, 2004. will be entered as indicated in the Advisory Action of January 27, 2005.

1. (Previously Presented) A thyristor device package having a cathode terminal and an anode terminal, comprising:

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

a first discrete metal oxide semiconductor (MOS) transistor connected in series with said thyristor between said cathode terminal and said thyristor emitter;

a second discrete MOS transistor connected between said cathode terminal and said thyristor gate; and

means for injecting current into said thyristor gate for triggering said thyristor into a latching state;

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a current to flow between said cathode terminal and said anode terminal turning said thyristor device package to an on state, and a zero to second voltage applied to said gate of said first MOS transistor turns said thyristor device package to an off state.

2. (Previously Presented) A thyristor device package as recited in claim 1 further comprising a floating ohmic contact (FOC) for shorting said emitter and a source terminal of said first MOS transistor.

3. (Previously Presented) A thyristor device package as recited in claim 1 further comprising a metal strap for shorting said thyristor emitter and a source terminal of said first MOS transistor.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. - 18. (Previously Canceled)

19. (Previously Presented) A thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal plate;

a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said thyristor device package;

a first discrete metal oxide semiconductor (MOS) transistor positioned on said second metal plate adjacent said thyristor, said first MOS transistor

having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for said thyristor device package; and

a second discrete MOS transistor positioned on said second metal plate adjacent said thyristor, said second MOS transistor having a first terminal connected to a gate of said thyristor, said second MOS transistor further having a second terminal connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns said thyristor device to an off state.

20. (Previously Presented) A thyristor device package as recited in claim 19, further comprising a clamp means for holding said first, second and third metal plates together.

21. (Previously Presented) A thyristor device package as recited in claim 19, wherein said first, second and third metal plates comprise copper plates.

22. (Previously Presented) A thyristor device package as recited in claim 19, wherein said first MOS transistor and said second MOS transistor are complementary.

23. (Previously Presented) A thyristor device package comprising:

a gate turn-off (GTO) thyristor comprising a thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a first plurality of discrete switching devices connected in parallel and arranged in a circular fashion around said GTO thyristor, a first terminal of respective ones of said first plurality of discrete switching devices connected to said thyristor emitter and a second terminal of respective ones of said first plurality of discrete switching devices connected to a cathode terminal of said thyristor device package; and

a second plurality of discrete switching devices connected in parallel and arranged in a circular fashion around said GTO thyristor, a first terminal of respective ones of said second plurality of discrete switching devices connected to said thyristor gate and a second terminal of respective ones of said second plurality of discrete switching devices connected to said cathode terminal of said thyristor device package,

wherein a first voltage applied to gate terminals of said first plurality of discrete switching devices turns said GTO thyristor to an on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate terminals of said first plurality of discrete switching devices turns said GTO thyristor to an off state.

24. (Previously Presented) A thyristor device package as recited in claim 23, further comprising:

a first metal plate forming said cathode terminal;

a second metal plate separated from said first metal plate by an insulation layer, wherein said GTO thyristor and said discrete switching devices of said first and second pluralities of discrete switching devices are positioned on said second metal plate, said first and second metal plates acting as a heat sink.

25. (Previously Presented) A thyristor device package as recited in claim 23 further comprising a third metal plate forming an anode terminal of said thyristor device package.

26. (Canceled)

27. (Previously Presented) A thyristor device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a diode.

28. (Previously Presented) A thyristor device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a diode connected in parallel with a capacitor.

29. (Previously Presented) A thyristor device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a Zener diode connected in parallel with a capacitor.

30. (Previously Presented) A thyristor device package as recited in claim 23 wherein said discrete switching devices of said second plurality of discrete switching devices comprise a transistor connected in parallel with a capacitor.

31. (Canceled)

32. (Canceled)

33. - 37. (Previously Canceled)

38. (Previously Presented) A thyristor device package including

a thyristor element having an anode terminal, an emitter terminal and a gate terminal,

a first discrete semiconductor switch connected in series with said emitter terminal of said thyristor element by a first terminal of said first semiconductor switch,

a second discrete semiconductor switch connected in series with said gate terminal of said thyristor element by a first terminal of said second discrete semiconductor switch; second terminals of said first and second discrete semiconductor switches being connected together, and

means for shorting said emitter of said thyristor element to a terminal of said first discrete semiconductor switch or for injecting current into said gate terminal for triggering said thyristor into a latching state;

wherein said first and second discrete semiconductor switches are arranged such that a signal of a first type applied to said first discrete semiconductor switch turns said thyristor element to an on-state and a signal of a second type applied to said first semiconductor switch turns said thyristor element

to an off-state, and

wherein at least one of said first and second semiconductor switches is constituted by a plurality of semiconductor devices.

39. - 44. (Previously Canceled)

45. (Previously Presented) A thyristor device package as recited in claim 1, wherein

a gate terminal of said second MOS transistor is connected to said cathode terminal.

46. (Previously Presented) A thyristor device package as recited in claim 19, wherein

said second discrete MOS transistor further includes a gate terminal connected to said third metal plate.